DFEA

CFT/CPS Axial Track Finder
Run IIB Upgrade

Design Specification
Engineering Note 2004-02-17a

PRELIMINARY

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1 Overview

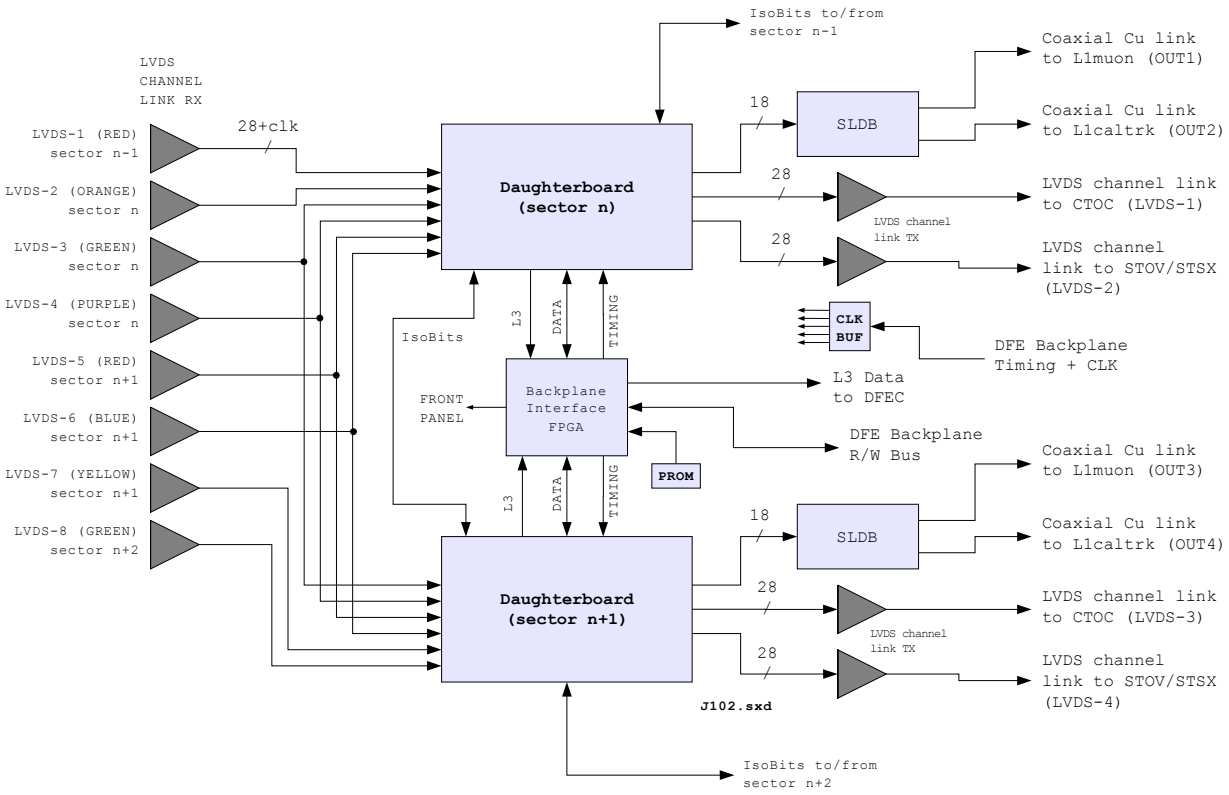
The original run IIA track finder boards consist of a pair of single-wide daughterboards (DFEA) mounted on a DFE motherboard (DFEM). This DFEA hardware and firmware is documented in the DFEA Technical Design Report [1]. This document is a companion piece to the original TDR; it describes important differences and improvements, such as:

- A new motherboard /daughterboard design.
- A new DFE crate controller with a faster connection to the D0 online computers.
- A new DFE backplane design (all cables enter through the backplane).
- No more transition boards.
- 48VDC power distribution.
- Improved diagnostics: input and output buffers.

Throughout this document the new upgrade board (including motherboard and daughterboards) will be referred to as the DFEA upgrade board.

An overview of the Central Track Trigger is available in the System Overview section of the CTT Online Homepage [2].

1.1 Block Diagram



2 Board Mechanical

The most significant change to the DFE crate is that now all I/O connects through the backplane as opposed to the front panel. Each board slot will have eight LVDS input cables and four LVDS output cables passing though the backplane. Also, each DFE board will have four coaxial cable outputs which also pass through the backplane.

2.1 Board Dimensions

The DFE board dimensions are 6U (233.5mm) x 320mm deep. While the backplane connectors are custom, the rest of the board specifications (spacing, max. component heights, etc.) should follow standard VME guidelines [3].

Refer to the DFE Backplane Specification [4] for the pinout of the backplane connectors. Also included on that website are mechanical drawings of the DFE board showing connector locations.

2.2 Front Panel

Since the input cables are now in the rear of the crate, the entire front panel is free for LEDs, test points, and programming connectors. *Refer to section 6.4 for details on the LEDs.*

2.2.1 Handles

The DFE backplane connectors have 300 pins and four coaxial connectors. To make insertion and removal easier, type HL (high leverage) handles should be used. Refer to Schroff documentation [3] for a drawing of the handles and front panel dimensions.

The front ejector rail on the DFE crate will provide a special overhang which the HL handles will latch onto. See the IEEE specification 1101.10; Schroff part number 30846-465 or equivalent.

2.2.2 Shielding

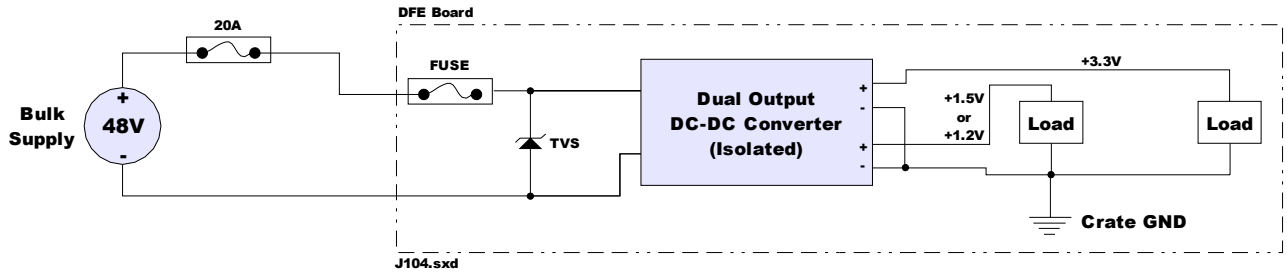
RF shield gaskets should be used on the side edges of the front panel. Refer to Schroff documentation [3] for part numbers and drawings.

2.2.3 Test Points and Connectors

The front panel should have a header to which a scope or logic analyzer can be connected. The signals going to this connector should come from the backplane interface FPGA. Specific signal definitions TBD. Also, the JTAG connector [REF] should also be accessible from the front panel; the JTAG chain should connect all FPGAs and the PROM for the backplane interface.

3 Power Distribution

The DFEA boards will be powered by a bulk 48VDC supply. An isolated DC-DC converter will generate the +3.3V and +1.5V (+1.2V for Spartan III) needed to power the logic on the DFEA board, as shown below:



The negative outputs of the isolated DC-DC converter should be tied to crate/rack GROUND through the backplane. Fermi Electrical Safety Guidelines [5] specify that a fuse and transient voltage suppressor (TVS) should be used on each board to protect the converter inputs.

The DFEA design may consume as much as +1.5V @ 15A and +3.3V @ 5A. A DC-DC converter such as the **QD48T015033** from **di/dt** meets these requirements. This converter is currently being studied to determine if radiated EMI is within acceptable levels.

4 High Speed Board I/O

4.1 LVDS Inputs from MIXER

The MIXER boards collect data and control bits from the AFE boards and repackage this information into L1 records which are sent continuously to the DFEA boards over the LVDS channel link cables. Each L1 record is 28 bits wide and 7 frames long (one frame per 53MHz RF clock tick). Record boundaries are denoted by the least significant bit, which is set to mark the LAST frame in the record – this is called the SYNC bit and it's present on each link.

LVDS input links 2 ("orange") and 6 ("blue") encode system control bits into the data stream. Refer to the DFEA Technical Design Report [1] for details on how these bits are encoded into L1 records.

The maximum allowable skew between any two input links on the ±1 RF clock tick.

The data bit ordering is different on each link with a group of 16 sectors (aka super-sector). Refer to the DFE Connections Homepage [6] for details on this mapping.

4.1.1 Test Pattern

Testing the data integrity on the LVDS links between the MIXER and the DFEA boards involves sending known test patterns over the links. This test is performed manually, usually after a board swap or cable check.

The MIXER boards can be put into a mode where they send a modified "walking 1's" pattern on all output links. Refer to the MIXER design specification [7] for details on the format of this pattern. It's important to note that when the MIXER is in test pattern mode the DFEA input links will no longer be synchronized, and no assumptions can be made about the relative skew between the links. The MIXER also encodes a relative sector number and link color fields into the test pattern. Checking these fields is optional – the original DFEA firmware design disregarded these fields.

4.2 LVDS Outputs to CTOC/STOV/STSX

The DFEA produces L1, L2CFT, and L2CPS records which are sent to the CTOC and the STOV/STSX boards. Currently the same information goes out on both outputs.

Refer to the DFEA TDR [1] for details on the output record formats. Also see the DFE Protocols Document [8].

4.2.1 Latency

Downstream boards require that their input records be synchronized, thus the DFEA design must have a fixed latency. Refer to the DFEA TDR [1] sections 5.7 and 6 for latency specifications and L1/L2 output record sequencing.

4.3 Outputs to L1muon and L1caltrk

Each sector must send the six highest Pt tracks to the L1muon trigger system. Each DFEA board contains two sectors, and thus two L1muon transmitter daughterboards (SLDB) are needed. Each SLDB board has two coaxial copper outputs. Refer to the DFEA TDR [1] section 5.3 for details. A few things are worth noting here:

1. The latency requirement for L1muon was the most stringent constraint in the original design. This requirement may be eased back for the upgrade, but to be safe the new DFEA board should try to keep the latency unchanged.
2. Currently there are three unused bits in each 16-bit word; L1caltrk may use these bits to send some additional track or cluster information TBD.

The L1muon SLDB interface consists of 16 data bits and two control bits: transmit_enable, and parity_enable, and a 53MHz clock. These control bits are tied to the master control bits that the DFEA board will now receive over the backplane. There is a specific sequence that must be followed during SYNC_GAPs and after an SCLINIT (aka CFT_RESET) is asserted. Details in the DFEA TDR section 5.3, and also in the DFEA VHDL firmware file *muon_top.vhd*.

4.4 Isolated Track I/O

Each trigger sector must inform its neighboring sectors if it has found one or more CFT tracks. This is necessary to determine if a track is isolated. This information is shared across dedicated lines on the DFEA board and backplane. The DFE Upgrade Backplane Specification [4] shows which backplane pins are used for these communication channels. Also refer to the DFEA TDR [1] section 5.4.6.

Note that the communication paths between DFEA boards are differential pairs, and LVDS drivers/receivers should be used here. Also, the firmware design should allow for propagation through the longest path – which is when the isolation data must be shared between crates through a 1m cable.

5 Clock and Control Bit Distribution

The original DFE boards received their clocks and control bits directly from the input data stream (*embedded control bits*). Since each DFE board would get multiple input links, typically one link was selected as the master link and that controlled the entire board.

The new DFEA boards will all get their master clock and control bits from a single source – the serial command link (SCL) receiver board. This board is located on the DFEC and the clocks and control bits are distributed over the backplane to all DFE boards. The control bits are serialized and sent to each DFEA board. Each DFEA board is responsible for "locking" onto this simple control bit frame format. *Refer to the DFE Crate Controller Specification [4] for more information.*

5.1 Control Bit Alignment

It is important to note that the master control bits will arrive at the DFEA boards ***some time before*** the corresponding embedded control bits – this is due to the latency of the AFE and MIXER boards. It is not known yet exactly what this offset will be, but it will probably be less than 50 RF clock ticks. The DFEA firmware must delay the master control bits so that they line up with the embedded control bits. This delay should be changeable via a write to a register. The smallest delay increment will be one RF clock (18.8ns).

The master control bits are more reliable than the embedded control bits. For this reason the DFEA boards will use these master control bits and clock exclusively for normal operation. However, the DFEA boards should compare the master control bits against the embedded control bits. If the embedded control bits disagree with each other or the master control bits, then it's an *upstream board problem* and DFEA boards should flag it as an error condition and continue to operate using the SCL control bits. Refer to the *Diagnostics section* for details on how to report these error conditions.

The most straightforward method of "dialing in" the master control bit delay would be to put a oscilloscope probe on the master FX control bit and another probe on one of the embedded FX control bits, and then write to a register to adjust the delay until the two pulses line up. While this technique will work well for commissioning during the shutdown, there should also be a mechanism by which this offset can be checked and adjusted remotely.

6 Link and Board Level Diagnostics

Many of the error conditions seen by the DFEA board will be momentary glitches, perhaps lasting only one RF clock tick. The original DFE firmware designs use "history bits" – that is, an error register that accumulates error conditions until it is explicitly cleared by the user. The following diagnostic bits should include a similar "history" feature.

6.1 Input Link Diagnostics

6.1.1 Link Clock

If an LVDS cable is unplugged the receiver's PLL will drift down and settle around 7MHz. The DFEA firmware should check the clock frequency of all input links and report any links which are not generating a 53MHz clock [8 bits].

6.1.2 Link Synchronization

All input links should be aligned to within 2 RF clock ticks. The DFEA firmware front end is responsible for cleanly and reliably crossing from the link clock domain to the master clock domain. If the input links are skewed badly enough then at some point the front end will not be able to realign them properly. The front end firmware should detect this condition by and report the bad links [8 bits].

6.1.3 Sync Bit Period

The SYNC bit is used for determining the beginning and end of the incoming L1 records. This bit should always be set one out of every seven clock ticks. If it is not, the bad link should be reported [8 bits].

6.1.4 Mixer Test Pattern

Data integrity between the MIXER and the DFEA board is checked by forcing the MIXER into a test pattern mode. The DFEA then checks this known pattern for bit errors. Links with bit errors should be reported [8 bits].

6.1.5 Embedded Control Bits

As mentioned previously, input links 2 and 6 have control bits embedded their L1 records. These control bits are FirstXing, SCLinit, SyncGap, and L1accept. The DFEA firmware must compare these embedded control bits against the master control bits (from the backplane). If there is any disagreement, the bad link(s) and bits should be reported. [8 bits].

6.2 Control Bit Status

A small finite state machine is used to "lock" onto the master control bits arriving over the backplane. Once locked onto the start bit, the state machine can expect to see the start bit every seven clock cycles. If for some reason the start bit is not observed at the proper time the state machine should be declared as "unlocked" and this is an error condition that needs to be reported.

When the state machine is locked to the control bits it should also be checking the odd parity bit. If there are any parity errors, this also needs to be reported [2 bits].

6.3 FPGA Status

The original DFE hardware was designed with the configuration control lines tied together for all FPGAs on the board (SelectMAP and slave serial modes). While this saved a few lines, it proved to be a disadvantage for the following reasons:

- If one FPGA needed to be reprogrammed, all FPGAs would have to be reprogrammed.
- If DONE did not go high it was difficult to figure out which FPGA was having problems configuring.

For these reasons, it is *strongly recommended* to use separate PROG and DONE lines for each FPGA on the DFE board. For each FPGA the status of the DONE, PROG, and INIT lines must be readable from the backplane registers.

6.4 Front Panel LEDs

The following LEDs are dedicated to the following functions:

- +3.3V
- +1.5V (or +1.2V)
- DTACK
- READY (all FPGAs are have DONE=1)

Many of the board level status bits must be observable from the front panel, however, many of them do not need to be viewed at the same time. In order to reduce the number of LEDs a multiplexed arrangement should be used.

For example, on each MIXER board there is a bank of 16 bi-color LEDs. Pressing a button on the front panel selects one of 16 display modes for this bank of LEDs; the meaning of each LED depends on the current display mode. Thus the MIXER can display 16 out of 256 status bits at any given time.

A bank of eight such LEDs should suffice for the DFEA board. The following display modes should be supported:

3. FPGA DONE bits (one LED for each FPGA; the default display mode)
4. Input Link Clock Detect [7..0]
5. Input Link Synchronization [7..0]
6. Input Link Sync Period [7..0]
7. Input Link Test Pattern [7..0]
8. Master Control Bits: FX, SG, L1accept, SCLinit; locked and parity error.
9. reserved
10. reserved

Where applicable the LEDs should be pulse stretched with a monostable to display momentary glitches.

7 System Level Diagnostics

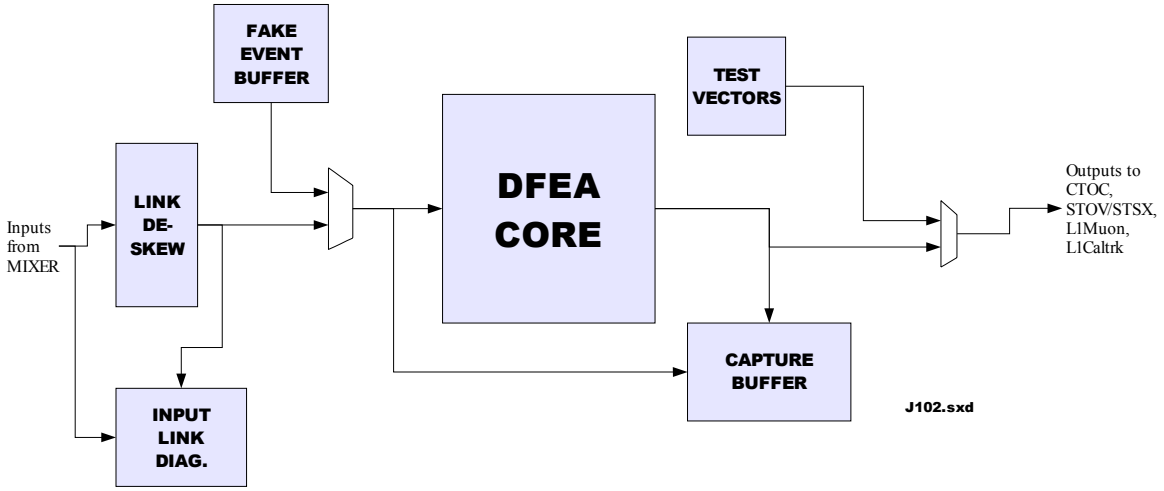
The purpose of the system level diagnostics is to make commissioning go as smoothly as possible. The functionality described in this section will enable the user to:

- Feed arbitrary test data into the design at full speed.
- Send test vectors downstream.
- Capture and read the input and output records.

Some of the features described in this section existed only on the bench, and required using a PC, a Datapump, power supplies, etc. Building system level diagnostic functionality into the production firmware has several advantages:

1. It reduces the need for custom test hardware (such as the Datapump).
2. Unlike a Datapump, it can be accessed after the boards are sealed in the collision hall.
3. The diagnostics evolve with the production firmware -- one does not have to support old special diagnostic firmware versions.
4. The diagnostic capture functionality can be accessed without interrupting dataflow.

7.1 Block Diagram



The block diagram above is a functional block diagram of the firmware modules for one sector.

7.1.1 Link Deskew

This module uses small dual port RAMs to cleanly cross from link clock domains into the master clock domain. The deskew module design is covered in the DFEA TDR [1] section 4.1.1.

7.1.2 Input Link Diagnostics

See section 6.1.

7.1.3 Fake Event Buffer

The fake event buffer will allow a user to load an arbitrary fake event or test pattern and inject it into the datastream at full speed as if it was real data coming from the MIXER. Switching between real input data and this fake event buffer should have no effect on the overall latency of the DFEA firmware design.

The fake event buffer should be readable and writable via the DFE backplane bus. Additional registers will control when this fake event buffer will get injected into the DFEA firmware core. The most useful modes will be:

- Continuous injection (repeat every 132ns crossing)
- Inject once per turn on a particular tick number (i.e. First Crossing)

Effectively, this *is* the Datapump board built into the DFEA firmware. Unlike a Datapump, however, this functionality can be activated at any time, whether the boards are on the platform or on the bench.

7.1.4 Capture Buffer

Normally, the downstream DFE boards will capture the DFEA board's output records and send them to the L3 readout crate. During bench testing and commissioning, this downstream hardware may not be available; the capture buffer provides a way to take a snapshot of the DFEA's inputs and outputs for an event. This buffer will be read out through the backplane bus.

This buffer should capture the input records as well as the L1, L2CFT, L2CPS, and L1muon output records. Several trigger modes should be supported:

- Capture the next event (triggered by a broadcast write operation to all boards on the backplane)
- Capture the next fake event (synchronized with the fake event buffer)
- Capture the next L1accept event.

7.1.5 Test Vectors

Being able to produce a known, fixed output record type is essential during the early stages of commissioning. All output record types (L1, L2CFT, L2CFT, and L1muon) should have at least one corresponding test vector record. When selected, these fake output records should be inserted into the datastream in such a way that the overall latency of the DFEA is not changed.

The DFEA TDR [1] sections 5.4.7, 5.5.2.3, and 5.5.2.5 specify the special output test modes for the L1, L2CFT, and L2CPS records, respectively. The new firmware design must implement these test records exactly to maintain compatibility with downstream hardware.

L1muon (L1caltrk) fake output records are defined as:

- Insert a fake maximum Pt track into the 10^{th} crossing; all other crossings get normal data.
- Replace the 16-bit data with two incrementing 8-bit counters; set the parity_enable bit low.

The details are in DFEA Muon Sender module (*muon_top.vhd*).

8 DFE Backplane Read/Write Bus

The DFE Crate Controller communicates with the DFEA boards over a simple A16 D16 bus. This bus is not VME, but rather it is a simple, synchronous bus who's clock rate is tied to the Tevatron beam crossing frequency (~7.5MHz). Refer to the DFE Crate Controller Specification [4] for details on bus signals and timing.

8.1 DFEA Backplane Registers

- Board Control and Status
  - Reset the board
  - Read/write the master control bit offset delay (see section 5.1)
    - Check that the embedded control bits are aligned with the master control bits
  - Master control bit status (locked and parity errors, see section 5)
  - Read/write the L2 pipeline depth.
  - Read the home sector numbers.
- Input Link Status
  - Multiple registers (see section 6.1)
- FPGA Registers
  - Each FPGA should have a separate PROG and DONE line.
  - Readback of FPGAs should be supported.
  - Readback a firmware version number (1 word) for each FPGA.
- Fake Event Buffer
  - Eight buffers, each is 14 words (memory map or FIFO?)
    - Readback the contents of the buffer.
  - Control registers for the Fake Event Buffer
    - Control when (or how often) injection occurs.
- Capture Buffer
  - Inputs: 8 x 14 words (memory map or FIFO?)
  - L1 out: 14 words
  - L2CFT out: 54 words
  - L2CPS out: 22 words
  - L1muon/L1caltrk out: 7 words
  - Control registers for the Capture Buffer
    - Setup trigger conditions.
    - Determine if a trigger has occurred.
- Test vector control registers
  - L1 output control.
  - L1muon/L1caltrk output control.
  - L2CFT output control.
  - L2CPS output control.
- Other registers TBD.

9 References

1. DFEA Technical Design Report
http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs/index.html

2. CTT Online Homepage
http://www-d0online.fnal.gov/www/groups/cft/CTT/online/ctt_main.html

3. Schroff Front Panel Express Design Guide (includes VME/eurocard specs)
http://www.schroffus.com

4. DFE Upgrade Hardware Specifications
http://www-d0.fnal.gov/~jamieson/run2b

5. Fermilab/DZERO Electrical Safely Guidelines
http://www-d0.fnal.gov/~hance/tools.htm

6. DFE Connections Homepage
http://www-d0online.fnal.gov/www/groups/cft/CTT/online/docs/interconn/connections.html

7. MIXER System Documentation
http://www-ese.fnal.gov/D0_CTT_MIXER

8. DFE System Protocols
http://d0server1.fnal.gov/projects/VHDL/General/

10 Revision History

17 Feb 2004: First draft.
24 Feb 2004: Removed L3 output; updated power supply; moved the backplane bus, clock and control bit stuff to the DFEC spec; added some register definitions/suggestions.